

Behavioral Modeling & Simulation of 2nd Order Current-Switched Charge Pump PLL Based Clock & Data Recovery Circuit

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Abstract

Many digital, clock, microprocessor, and wireless gadgets employ clock and data recovery circuits (CDR). It is preferred to acquire without using a reference clock in order to save money on the receiver's expensive crystal oscillator. In this publication, a clock and data recovery circuit (CDR) based on a 2nd-order current-switched charge-pump phase-locked loop (CSCP-PLL) is designed. No external components were used to generate the CDR. When the input data is non-zero prior to the locking point, the system enters into quasi-harmonic transient mode, and the phase error reaches a fixed value, exposing a highly chaotic region. Because the CP-PLL is a mixed-signal system consisting of analog and digital blocks as well as low and high frequencies, the linear theory of feedback system cannot be applied to sampled and non-linear characteristics. Alexander phase detector, current-switched charge-pump (CSCP), analog loop filter, and linear voltage-controlled oscillator are used to analyze the behavioral model of the CSCP-PLL-based CDR loop. Simulation results show that the clock and data are flawlessly retrieved at the intended frequencies. The findings of this research are: Total Jitter= 25.20ms, RMS Jitter= 10.25ms, Signal-to-Noise Ratio= 2.08 (unit-less), Q-Factor= 154.45 (unit-less), Rise Time= 10.80ms, Fall Time= 10.40ms, Eye-Level= -0.67 V, Vertical Opening= 0.02 V, and Horizontal Opening= 14.80ms. Also, the model comparison and validation are discussed.

Keywords—CP-PLL, CDR, Clock, Data, Alexander Phase Detector, Current-Switched Charge Pump, Loop Filter, VCO

1 Introduction

The most common applications for CDR circuits are in control, digital, clock, microprocessor, and communications [1], [2]. The CDR serves as an essential component of all serial communication systems, recovering the clock and retiming the incoming data [1]. As determined by the jitter tolerance (JTOL) parameter, it must accept input jitter and successfully recover data without errors. The clock and data recovery circuits (CDR) are preferred to acquire data without using any reference input [3] and hence save the cost of the receiver's (Rx) most expensive crystal oscillator [4], [5]. In this publication, a clock and data recovery circuit (CDR) based on a 2nd-order current-switched charge-pump phase-locked loop (CSCP-PLL) is designed [6]. Nothing external is used to generate the clock and data [7]. In a typical CDR, the voltage-

controlled oscillator (or VCO) generates the clock as illustrated in Fig. 1. The difference in phase between the two inputs, when the phase of the input data to clock is compared using a phase detector, generates the error signal. Then the charge pump and loop filter are driven by the phase detector (up and down) signals to produce the oscillation control voltage (V_{ctrl}) [8]. Although the clock signal drives a decision circuit, it retimes data and reduces its jitter [9]. Because the CP-PLL is a mixed-signal system that contains both low and high frequencies, the linear theory of feedback systems cannot be applied to sampled and non-linear characteristics [10], [11], [12]. Consequently, the CDR loop's behavioral model is created.

2 Materials And Methods

Fig. 1 shows the overall design of the CSCP-PLL-based CDR circuit, and the following paragraphs go into further depth about each system-level component:

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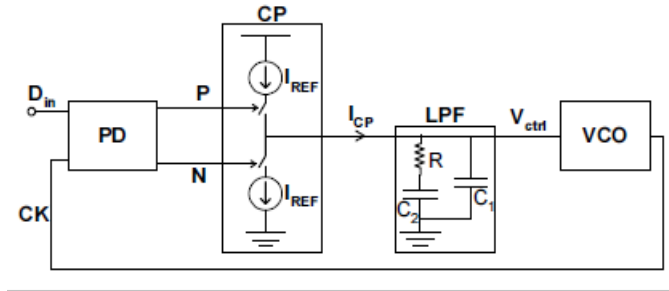


Fig. 1: The General CDR Architecture [13], [14]

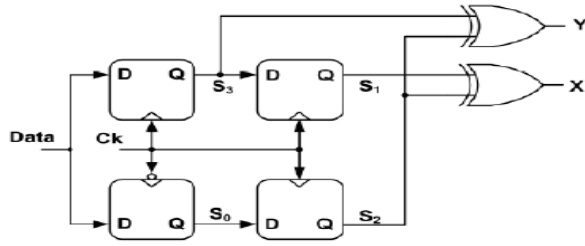


Fig. 2: Alexander Phase Detector [15]

2.1 Alexander Phase Detector

This is the most widely used phase detector. It consists of two data mock-ups and one edge mock-up. Fig. 2 depicts the Alexander phase detector model. As illustrated in Fig. 3, the PD with three mock-ups can access about a data transition on time, and the clock (leading) is early or late (lagging).

All samples are the same if there are no transitions; hence nothing happens. The 1st mock-up S_1 doesn't equal the other two mock-ups if the clock is leading. If the first two mock-ups, S_1 and S_2 , are the same, the clock is lagging, while S_3 is different. As a result, the XOR of the pairings $S_1 \oplus S_2$ is ON and $S_2 \oplus S_3$ is OFF. This indicates that the clock is late. The clock is early if $S_1 \oplus S_2$ is OFF and $S_2 \oplus S_3$ is ON. If $S_1 \oplus S_2$ equals $S_2 \oplus S_3$, then nothing happens.

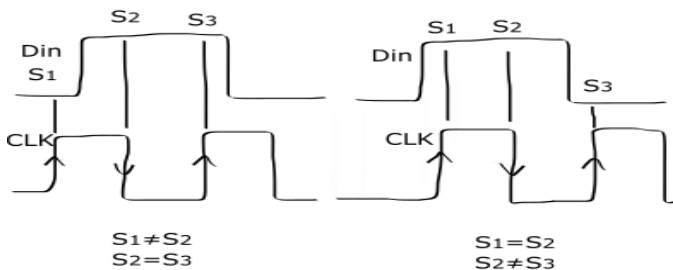


Fig. 3: Early Late Clock Definitions [16]

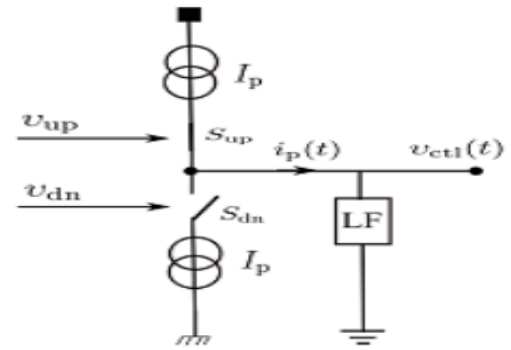


Fig. 4: CSCP circuit with an RC Filter [17], [18], [19]

2.2 Current-Switched Charge Pump

A current-switched charge pump (or CSCP) is a current source or sink that, depending on its inputs, charges/discharges the loop filter. The primary concept is to keep a constant flow of current that only switches directions when necessary. Peaking during transitions is reduced in this way. The up and down signals of the Alexander phase detector are inputs to the charge pump (or CP). The CP converts the phase detector up and down signals into pump current signals (I_p) that turn ON/OFF the current source and sink of the charge pump. Fig. 4 depicts the CSCP circuit with the loop filter configuration.

Two transistors are utilized as switches in this CSCP design, and the CSCP operates in up and down cycles. It can be expressed as follows [20]:

$$I_p = \begin{cases} +I_p, & \text{Up State} \\ 0, & \text{Null} \\ -I_p, & \text{Down State} \end{cases} \quad (1)$$

The analysis of CSCP's transient behavior is less complicated than that of a voltage-switched charge pump (i.e., VSCP) because the CSCP-PLL architecture consists of symmetrical pump current characteristics. The CSCP design uses two complementary constant current sources to deliver zero current during the high impedance state and an ideal constant pump current I_p throughout every PD transition cycle. Hence, the gain associated with the phase detector (K_{pd}) remains constant [17], [18]. [20].

2.3 Loop Filter

The objective is to discard higher-order frequency harmonics from the PD output. In essence, the loop filter circuit is a series network of RC (resistor x capacitor) passive components as illustrated in Fig. 5. The result

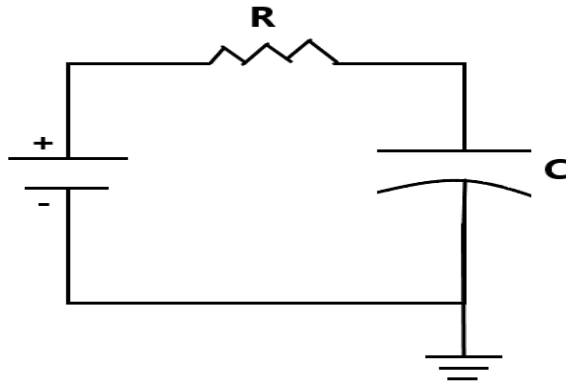


Fig. 5: Loop Filter [19]

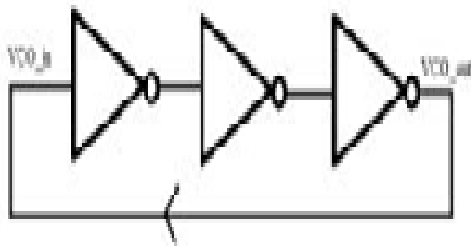


Fig. 6: Ring Oscillator [18]

of the loop filter is in volts (i.e., the control voltage V_{ctrl}) as input to the VCO. While creating a quasi-DC signal that accelerates or decelerates the VCO, a correction signal is provided to the loop filter when a phase detector detects the phase error. The V_{ctrl} is generated by charging/discharging a capacitor in the loop filter circuit. The operation of CP-PLL is stabilized by the filter impedance. Due to the loop filter impedance, a non-linear phenomenon such as frequency excursions occurs in 2nd-order CP-PLLs.

2.4 Voltage Controlled Oscillator

Being the engine of PLL, it produces a signal whose angular frequency is relative to V_{ctrl} at its inputs [21]. The VCO architecture based on CMOS technology is the classical ring oscillator (Fig. 6).

The VCO is cascaded with looped cells in which each inverting cell introduces a functional delay. The VCO output signal's acceleration and deceleration are controlled by V_{ctrl} since it adjusts the delay of each inverter. An output signal is produced by a VCO depending on its V_{ctrl} . The frequency of the output voltage is directly related to V_{ctrl} . The loop filter is V_{ctrl} . The VCO produces an output with a greater frequency as the V_{ctrl} increases and vice versa. The voltage V_{ctrl} becomes unchanged in the locked state of

the system, which also fixes the oscillation frequency of the VCO clock.

2.5 Why Choosing CSCP-PLL over VSCP-PLL

PLL Model can be designed using either a voltage-switched charge pump (VSCP) or a current-switched charge pump (CSCP).

- 1) CSCP uses a constant current source, which is not the case for VSCP.
- 2) CSCP delivers the constant pump current (I_p) ideally during each transition cycle of the phase detector, which is not possible in the case of VSCP.
- 3) In the linear mode of VSCP-PLL, the transfer function is a bit more complex as compared to CSCP-PLL. This is why the CSCP-PLL system is more reliable and stable than VSCP-PLL.
- 4) VSCP-PLL undergoes a peculiar effect.
- 5) The analysis of CSCP's transient behavior is less complicated than that of a voltage-switched charge pump (i.e., VSCP) because the CSCP-PLL architecture consists of symmetrical pump current characteristics. The CSCP design uses two complementary constant current sources to deliver zero current during the high-impedance state and an ideal constant pump current I_p throughout every PD transition cycle. Hence, the gain associated with the phase detector (K_{pd}) remains constant [17], [18]. [20].
- 6) Consequently, designing the CSCP-PLL is more robust and accurate (higher efficiency).

In this publication, the behavioral modelling and simulation of a 2nd-order current-switched charge pump PLL (CSCP-PLL) based Clock and Data Recovery Circuit (CDR) is developed using the Alexander phase detector, current-switched charge pump, analog loop filter, and a linear VCO.

2.6 Methodology

In this work, the behavioral modelling and simulation of a 2nd-order Current-Switched Charge Pump PLL-based Clock and Data Recovery Circuit (CDR) is developed using an Alexander phase detector, a current-switched charge pump (CSCP), an analog loop filter (LF) and a linear VCO. The behavioral model is designed, completed, and simulated throughout the steps as mentioned in the model methodology approach (fig. 7) using MATLAB & Simulink (fig. 8).

3 Results and Discussions

In this work, the behavioral model of a 2nd-order current-switched CP-PLL-based CDR was developed

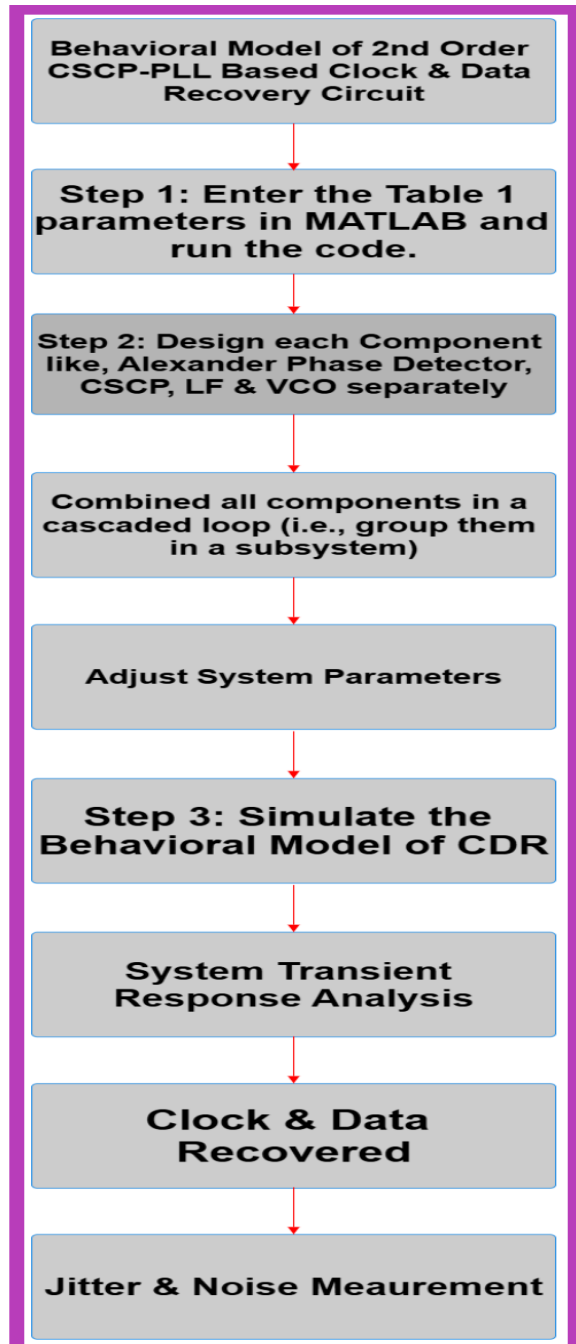


Fig. 7: Behavioral Modelling Approach

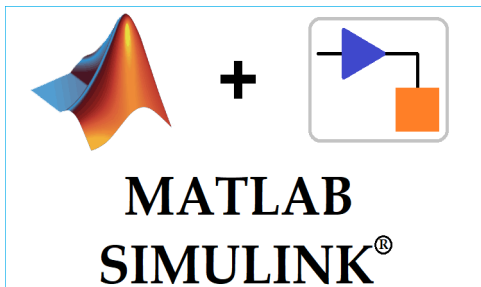
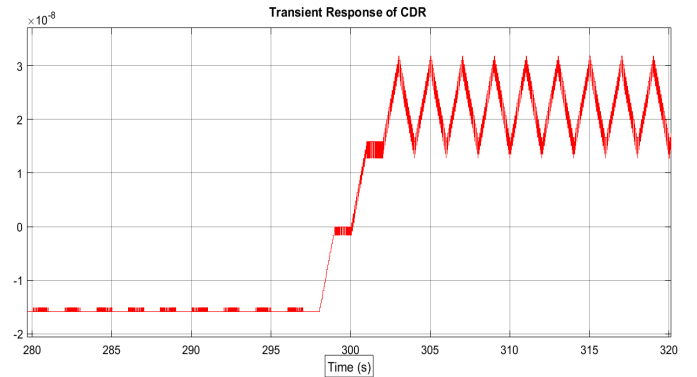


Fig. 8: MATLAB & Simulink Tool

TABLE 1: Clock and Data Recovery Circuit (CDR) Parameter Specification

S. No	Component	Notation	Value
1.	Recovered Clock Frequency	C_{freq}	100 MHz
2.	Recovered Data Frequency	D_{freq}	200 MHz
3.	Previous Frequency	EX_{freq}	0.5 MHz
4.	Charge Pump Current	I_{cp}	200e-6 A
5.	VCO gain	K_{VCO}	10
6.	Sampling Time	T_s	0.01 sec



caption CDR's Transient Response

using an Alexander phase detector, a current-switched charge pump, an analog loop filter (LF) and a linear VCO. Table 1 shows the parameter specifications for the model. The eye-diagram values are also measured (Table 2). The system's transient response behavior of each component, recovery of clock and data, the system jitter, and system noise (mentioned below) were analysed.

3.1 System Level Response

Fig. 9 shows that, before the locking point, a very chaotic area is revealed.

Due to this, there is a huge phase error. That phase error converges to a fixed value when the system locks, entering a quasi-harmonic transient mode as shown in Fig. 10.

At this point, the recovered clock and VCO signals are in phase as pictured in Fig. 11.

These clock and VCO signals drive the phase detector so as to generate the phase detector signals (up and down) as shown in Fig. 12.

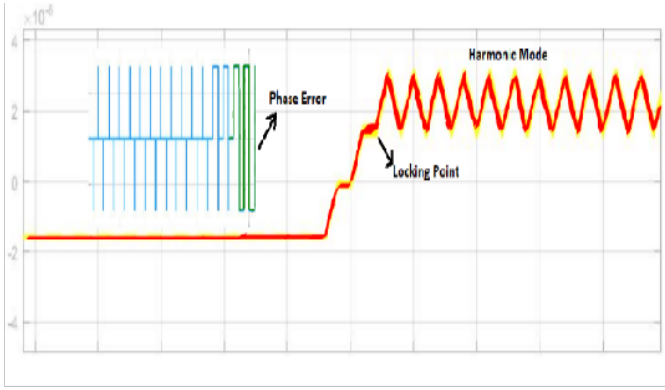


Fig. 9: Highlighting the Transient Response Zones

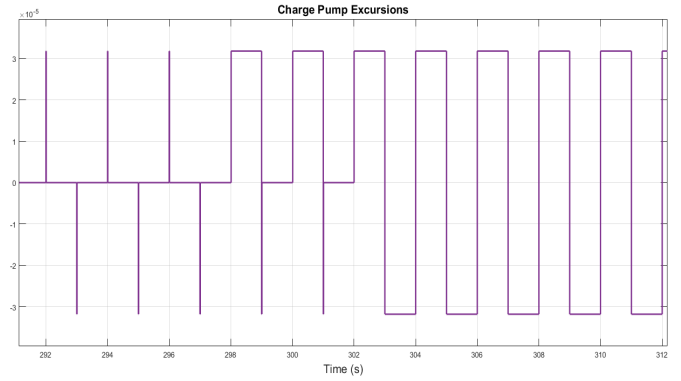


Fig. 12: Current-Switched Charge Pump Ripples

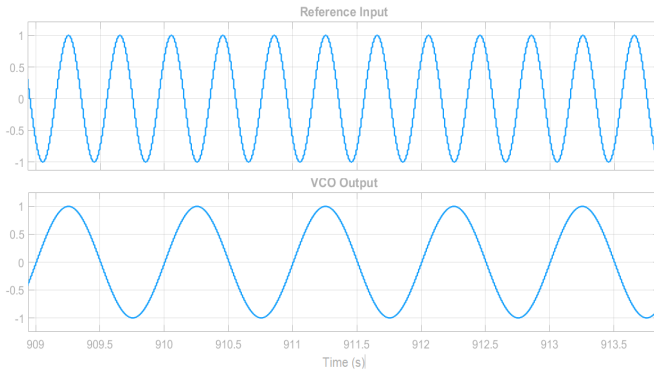


Fig. 10: The recovered Clock (i.e., reference input) and VCO output

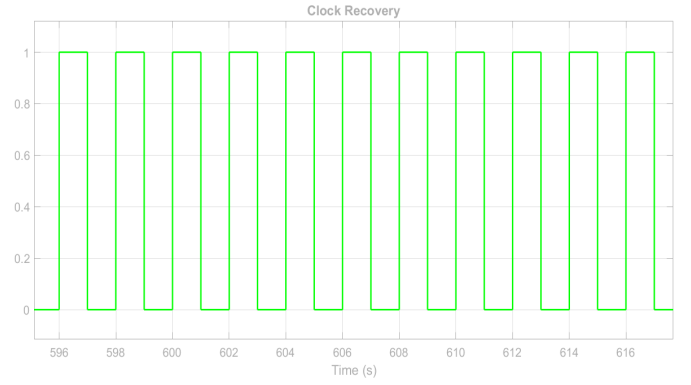


Fig. 13: Clock Recovery

Similarly, these up and down signals drive the current-switched charge pump (Fig. 13), which produces the symmetrical pump current signals.

The CSCP operates on only 00 and 01 Boolean numbers, so it provides the ripples based on the input signals as shown in Fig. 13. Finally, the loop filter (driven by pump current signals) produces the oscillator control voltage V_{ctrl} to tune the VCO. Fig. 14 shows that the clock is recovered at the desired

frequency.

3.2 Clock and Data Recovery

In this work, the behavioral model of a 2nd-order current-switched CP-PLL-based clock and data recovery circuit was developed utilizing the Alexander phase detector, current-switched charge pump, loop filter, and VCO. Fig. 14 and Fig. 15 show the CDR clock and data recovery signals recovered from the selected input data. This clearly shows that a clock can be recovered for a desired frequency and data can also be recovered at any desired frequency. Hence, it is proved that the designed model of clock and data recovery based on CP-PLL is perfect and works most accurately.

4 Jitter and Noise Analysis

The system's noise and jitter are the main assets of the clock and data recovery circuit.

4.1 Jitter Analysis

As jitter is the most important aspect of CDR, it affects the transfer of data from a receiver to a transmitter in the case of a CDR with an SERDES link.

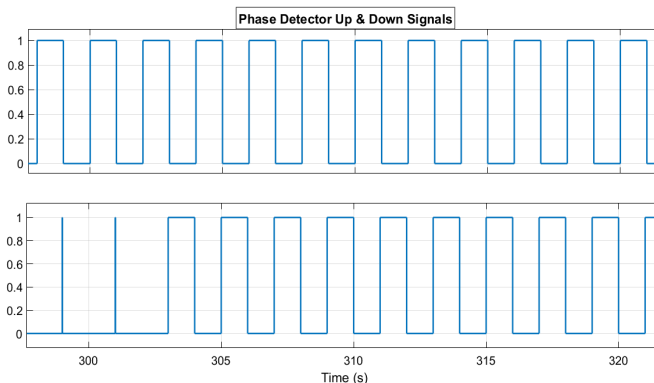


Fig. 11: Phase Detector Up and Down Signals

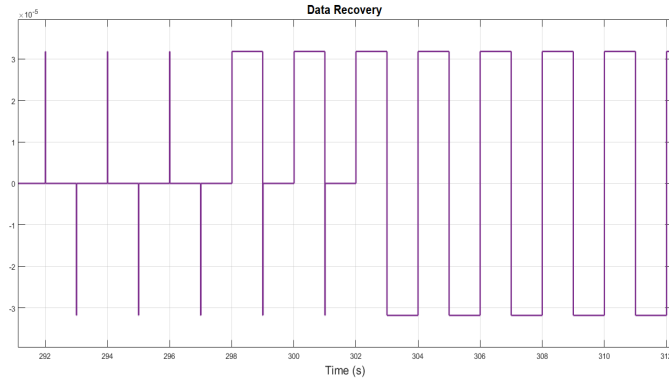


Fig. 14: Data Recovery

A good CDR system must exhibit less jitter. The recovered clock removes or reduces the jitter. The total jitter of our developed behavioral model is 25.20 ms. The random jitter is 0.00, and the RMS jitter is 10.25 ms.

4.2 Noise Analysis

The noise is an unwanted signal. Due to this noise, the data being transferred is distorted. This is why there should be less noise. The signal-to-noise ratio of our developed behavioral model is 2.08 (unitless).

5 Comparative Validation

5.1 Comparison of this model with [19]

In this research, the behavioral modelling and simulation of a 2nd-order current-switched charge pump PLL (CSCP-PLL) based clock and data recovery circuit is developed using an Alexander phase detector, current-switched charge pump (CSCP), analog loop filter, and a linear voltage-controlled oscillator (VCO).

- 1) In this paper, the VCO output with reference input is totally in phase; the phase error is minimized. The smaller the phase error (output of the phase detector), the more reliable and stable the system. The phase error is minimized compared to that of [19].
- 2) The system stability is optimized.
- 3) Moreover, the harmonic mode locking between the VCO output and reference input is more constant than that of [19].

5.2 Validation

In this publication, the behavioral modelling and simulation of a 2nd-order current-switched charge pump PLL (CSCP-PLL) based clock and data recovery circuit is developed using an Alexander phase detector,

current-switched charge pump (CSCP), analog loop filter, and a linear voltage-controlled oscillator (VCO). The validation points are mentioned as follows:

- 1) Clock signal has been generated (Fig. 14).
- 2) Data signal has been generated (Fig. 15).
- 3) Lesser phase error than [19] (fig 10).
- 4) Harmonic mode is exposed in the transient response analysis (Fig. 9 and Fig. 10), which proves the system reliability and stability.
- 5) The reference input and VCO output are in phase; the phase error converges to zero at the locking point.

6 Conclusion

In this paper, the behavioral modelling of a 2nd-order current-switched CP-PLL-based clock and data recovery circuit (CDR) was developed using an Alexander phase detector, current-switched charge pump, analog loop filter, and a linear VCO. Results reveal that before locking, a highly chaotic area was exposed, and that the system is now convergent to the target value via an average-harmonic transient mode. The clock and data are recovered with desired frequencies. Moreover, the jitter and noise were analysed. The findings of this research are as follows:

- 1) Total Jitter= 25.20 ms
- 2) RMS Jitter= 10.25 ms
- 3) Signal-to-Noise Ratio= 2.08 (unitless)
- 4) Q-Factor= 154.45 (unitless)
- 5) Rise Time= 10.80 ms
- 6) Fall Time= 10.40 ms
- 7) Eye-Level= -0.67 V
- 8) Vertical Opening= 0.02 V
- 9) Horizontal Opening= 14.80 ms

7 Future Scope

The future scope of CDR based on CP-PLLs is very vast regarding different modeling techniques, such as the behavioral model of a 2nd-order CSCP-PLL-based CDR can be analysed using:

- 1) Graphical user interface (GUI)
- 2) Event-driven (ED) approach
- 3) Monti-carlo simulations
- 4) Stability analysis using Lyapunov's stability method.

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