Minimizing Transmission Distortion in Parallel Concatenated Convolutional Codes with Constraints in Power and Bitrate

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Abstract

Wireless channels are prone to many impairments, which can cause the reception of erroneous packets on Weak channels. Weak channels can cause a high number of retransmissions in order to deliver a packet correctly, which will consume high energy from both the transmitting and receiving nodes. In this study, a solution is proposed for the allocation of power in Parallel concatenated convolutional coding (PCCC), and the Effect of bit rate and power on interleaved size and the effect of bit rate and power on encoder complexity have been presented and discussed. A strategy is developed for supply voltage levels for the encoding process and the interleaving process. Based on the strategy derived, it has been shown that the assignment of supply voltage levels minimizes the transmission distortion.

Keywords—Bit Rate, Dynamic Voltage Scaling, Parallel Concatenated Convolution Codes

1 Introduction

All modern digital systems designs are constrained by power [1]. The On-chip power is now becoming the prime design constraint. It is because of VLSI that a huge number of transistors on a single chip have played a vital role in making power one of the leading constraints. Systems in which the number of transistors is greater consume more power, whether in standby or during switching (Dynamic power), as compared to smaller systems used in the past [2]. The main sources of power dissipation are due to reverse bias current, sub-threshold current due to inversion charge below the threshold voltage, the DC standby current, the DC rust-through current between power rail supplies, and the capacitance current due to capacitive load during the change of logic [3]. The significance of the conservation of power increased even further with the advent of portable/mobile devices [4]. A most desirable property in mobile/portable devices is the extended battery lifetime, which is even more important than performance. Both design-time and runtime solutions can be used to reduce power consumption in such a way that it has a minimum effect on the performance of the system. Many solutions are available in the literature [5, 6]. The efforts made at design time yield greater improvements.

In runtime solutions, Dynamic-Voltage-Scaling (DVS) has been used quite extensively, in which the supply voltage is varied based on the computational load, and hence battery timings can be improved with it. Our research employs DVS in order to make variations in power levels during computations.

Smart sensors are widely used nowadays, and their applications in social life, military, biomedical, wildlife, and many other fields are numerous. The smart sensors must have accuracy and precision in their results, but must also utilize their resources to the best. The sensor's main task is to measure or sense some parameters and transmit the information to an aggregating node (usually wirelessly). The transmission of data (through the channel) must be efficient, and the sensor must be designed so that it does it efficiently under any of the constraints imposed upon it. Channel coding has great importance in wireless transmission. The most

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commonly used scheme for channel coding is perhaps turbo codes. Many types of encoders can be used with turbo codes, but in our work, we have the main focus on parallel concatenated convolutional codes (PCCC) because the performance analysis of PCCC is comprehensively documented, and the second reason is that its implementation is simple as based on mod-2 additions and shift registers. The power consumption by PCCC is also low compared to other coding techniques [7-9].

The on-chip power consumption values, as compared to transmission power, were previously very high, as conventional electronics consumed more power than today's electronics. However, the transmission and computational power have become comparable with the advent of ultra-low-power designs, particularly in small networks. It is usually the same battery that supplies the power to both (transmission as well as computation), so it becomes very important to develop such a strategy that allocates optimum power values to both of them. The channel coding is considered to be the computational load in our work. Now, if we allocate more power to the encoding process, we will obtain higher efficiency in the form of low bit error rates; however, under power constraints, less power is left for the transmission process, and hence efficiency is reduced. The main purpose of our research here is to develop a design-time strategy for power allocation between wireless transmission and channel coding in order to minimize the bit-error rate (BER).

The authors in [10] present a Reed-Solomon encoder that is dynamically configurable, i.e., according to the channel SNR, the encoder configuration is changed. In modern channel coding to PCCC PCCC-based codes (Turbo codes) are commonly used as compared to RS codes. In [11], the authors present a strategy that reduces the energy consumption and also reduces the delay for forwarding-sensor nodes employing rate 1/3 PCCC-based turbo codes. Power-optimized channel coding using LDPC codes is provided in [11]. In [12, 13], different coding schemes are analyzed at the circuit level is performed and their results show that Turbo codes outperform all other coding schemes in low-power scenarios.

The other sections of this paper are organized as follows. Section II of the paper discusses the different distortion sources in PCCC-based communication. Section III describes the results and discussion, where Section III. A describes the interleaved computational power effect, and Section III.B explains the encoder complexity effect. The minimal distortion power allocation is discussed in Section III.C. The conclusion of the paper is given in Section IV.

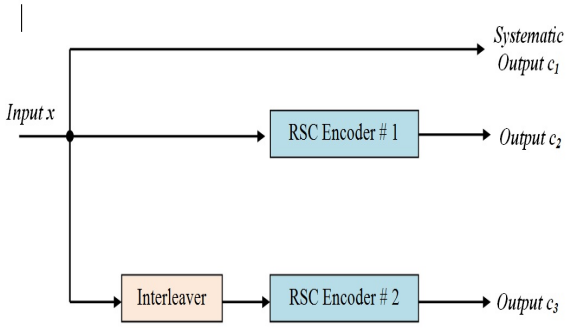

Fig. 1: Block diagram of PCCC

2 Distortion Control Parameters In PCCC

Turbo codes were presented by Berrou et al in [10] with improved performance compared to the earlier coding scheme. In turbo codes, the data is encoded by multiple constituent encoders at the transmitter end. The input (x) enters the 1st encoder interleaved, whereas it enters the 2nd encoder after performing interleaving by the interleaver. The two-component encoders are separated by an interleaver. The output, as can be shown, depends on the input (x) and the outputs of the two encoders. In general, two similar encoders are used in parallel. A fundamental turbo encoder is shown in Figure 1.

In [14], the bit-error performance analysis of turbo codes was performed by Benedetto et al. The maximum bit-error rate for a turbo coding scheme based on PCCC was presented in [9] and is given by:

$$P_b(e) \leq \sum_{k=1}^{[N/2]} 2k \binom{2k}{k} N^{-1} \left. \frac{(H^{2+2z_{min}})^k}{(1-H^{z_{min}-2})^{2k}} \right|_{H=e^{-R_c E_b/N_0}} \quad (1)$$

The minimum weight of the parity bits for a weight-2 input to one of the constituent encoders is denoted by z_{min}, N shows the interleaved size, and R_c shows the code rate. It is assumed that the interleaver performs uniform random permutations of the input data. For the turbo codes, the choice of code rate is based on the available bandwidth. In this work, we will not deal with the code rate as our focus is on the system bit rate and power. In this paper, results are provided for different bit rates. The computational load of the system is comprised of the interleaver process and the encoding process, while the energy per bit is determined by the transmission power. This research presents Dynamic Voltage Scaling (DVS) for the system to control the computational power. Due to some reasons, Dynamic Voltage and Frequency Scaling (DVFS) is not used. First, the on-chip core frequency

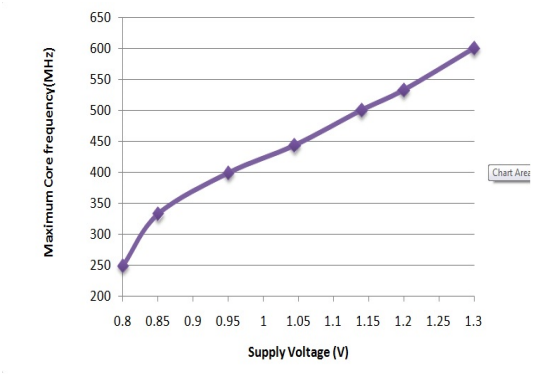

Fig. 2: Synchronous reluctance motor view of stator and rotorSupply voltage (v_{dd}) vs max core frequency (f_{max}) for BF-537

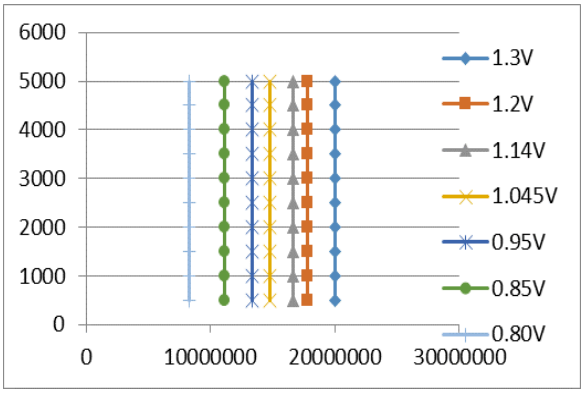

Fig. 3: Random interleaver Data rates and their corresponding sizes

varies with the supply voltage, so the maximum core frequency of the system varies with a change in supply voltage. Thus, the change in power is more than the square law. Secondly, we consider the constant bit rate because the sensor load is normally constant, and it transmits continuously; thus, there is no need to change the frequency at runtime. Simply put, the core frequency varies with changes in supply voltage according to the specified ratings, so the focus is on a single variable, i.e., supply power. The complexity of the computational process depends on constraints imposed by power and the bit rate. Computationally complex tasks can be performed at high available power and lower required bit rate, and vice versa. For a process, the achievable complexity is expressed as:

$$C(\phi) = h(R_{b_{max}}, P_{max}) \tag{2}$$

For a process, the on-chip power consumption can be calculated by:

$$P = \alpha v_{dd}^2 f \tag{3}$$

Where the value of α depends on several factors and is f constant, v_{dd} is the core clock frequency of the system, and is the voltage supplied to the system. At f_{max} (the maximum clock frequency of the core) operated at voltage v_{dd}, the maximum power consumed by the system is

$$P_{f_{max}} = \alpha v_{dd}^2 f_{max} \tag{4}$$

The above equation f_{max} is the maximum core frequency and strongly depends on the power supply. The value f_{max} is usually provided by the vendors in data sheets. We had used $DSP(BF-537)$ in our experiments. The relationship between the supply voltage (v_{dd}) and maximum core frequency (f_{max}) for DSP-537 is graphically depicted in Figure 2 below.

Mathematically,

$$f_{max} = g(v_{dd}) \tag{5}$$

The function is not fully linear but piecewise linear in some regions. The frequencies vary linearly in voltage above 0.85, i.e., in the range of 0.85 to 1.3 volts. It can be modeled by the following equation:

$$f_{max} = 5.784 \times 10^6 v_{dd} - 1.564 \times 10^8 \tag{6}$$

3 Results and discussion

3.1 Effect of Bit rate and power on interleaved size

The bit rate has no relationship with the size of the interleaver. It only affects the delay of the interleaver, which increases with an increase in the size of the interleaver, but it also increases the number of interleaved bits. Thus, the computational complexity does not increase at the transmitter node. For decoding, the actual encoded data and interleaved data should arrive at the same time, so the transmission module must wait for encoded interleaved data so that it can send it along with encoded non-interleaved data. Thus, the increase in size of the interleaver increases the initial delay in the decoding process. Increasing the level of power for interleaving increases the core frequency (section II), which will affect the bit rate of the interleaving process. So it can be easily concluded that bit rate depends on the amount of supply and the constraint of power allocation, and bit rate does not affect the size of the interleaver. Both a random interleaved and the conventional UMTS interleaves described in the experiment are shown to have maximum bit rates and matching interleaver sizes [15].

The results shown in Figures 3, 4, 5, and 6 clearly indicate that the size of the interleaver is independent

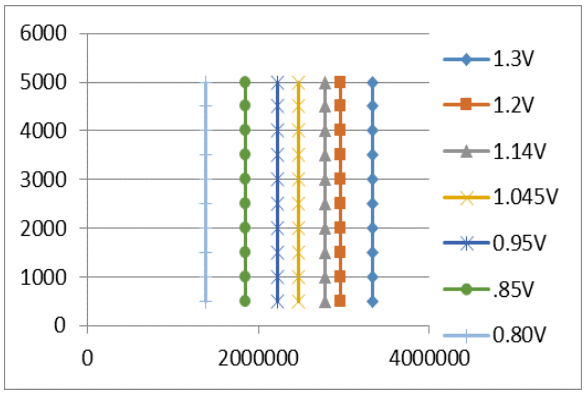

Fig. 4: TTI 20ms interleaver Data rates and their corresponding sizes

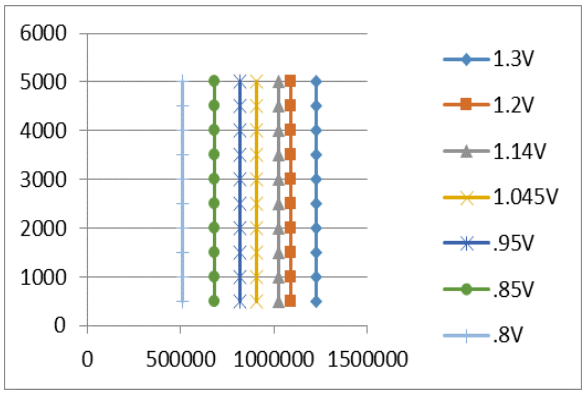

Fig. 5: TTI 40ms interleaver Data rates and their corresponding sizes

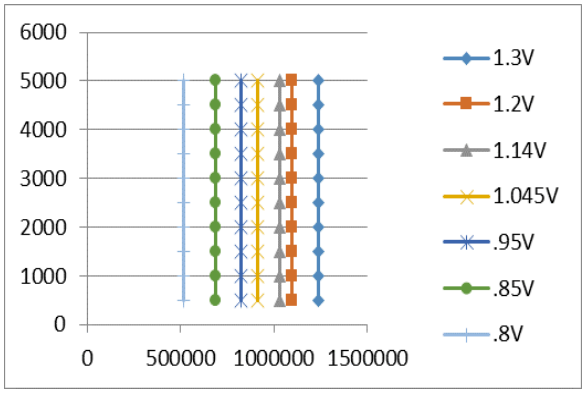

Fig. 6: TTI 80ms interleaver Data rates and their corresponding sizes

of allocated power and bit rate. As aforementioned, bit rate depends on supply voltage, i.e., power.
The change in the supply voltage affects the bit rate as discussed above. This change in supply voltage corresponds to the change in maximum core frequency. So the bit rate depends on the core-clock frequency also, which can be modeled by the following equation:

$$R_b = \beta f_c \tag{7}$$

Here β is a constant, and is equal to M number of bits to be processed in x number of cycles, which is represented by the following equation:

$$\beta = \frac{M}{x} \tag{8}$$

3.2 Effect of Bit rate and Power on Encoder Complexity

For weight-two input, the minimum output distance (z_{min}) depends upon the encoder's complexity. When the encoder's complexity is greater, the value of (z_{min}) is also greater, and vice versa. The complex convolution encoder has a greater value of (z_{min}), but it will cost more computational power and delay. In other words, simple convolution has a small delay and consumes less power as compared to a complex one. For Turbo codes, the effective free distance is given by [16]:

$$d_{free,eff} = 2 + 2zmin \tag{9}$$

The effective free distance is an important parameter for convolutional codes. Turbo codes with component en-coders (Recursive) they must be chosen to maximize (z_{min}) and also maximize the $d_{free,eff}$. A number of convolutions have been discussed in [17], which are being optimized on a minimum output weight basis with a given size of input weight, as well as on multiplicities. In this work, the encoders presented in [17] are used because they give higher performance compared to the encoder given in [12]. Our analysis has been performed on ($rate = 1/n$) encoders only because in most environments they will serve the purpose. However, similar models may be developed for other types of encoders that are presented in [12].

A mathematical model for an encoder having a 1/4 code rate is not simple; thus, it has not been derived, while for a 1/3 coding rate, the mathematical model for the encoder is represented by the following equation.

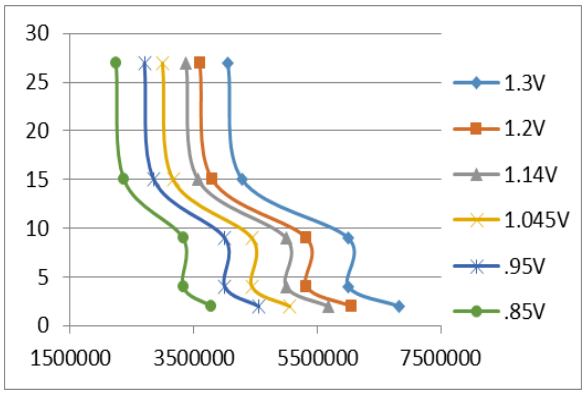

Fig. 7: 1/4 PCCC Data rates and their corresponding achievable z_{min}

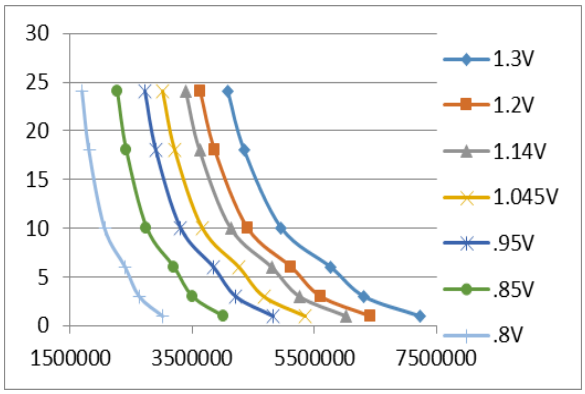

Fig. 8: 1/3 PCCC Data rates and their corresponding achievable z_{min}

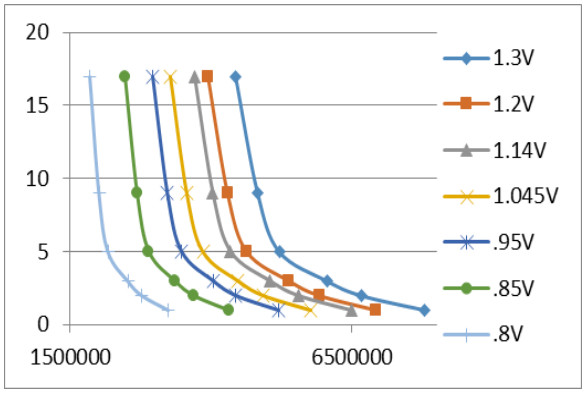

Fig. 9: 1/2 PCCC Data rates and their corresponding achievable z_{min}

$$z_{\min}^{1/3}(R_b, f_{\max}) = \begin{cases} 31.43\, e^{\frac{786.72}{f_{\max}}(R_b - 0.0068 f_{\max})} & \text{where } 0.0068 f_{\max} \\ & \leq R_b \leq 0.012 f_{max} \\ 0 & \text{else.} \end{cases} \tag{10}$$

For a 1/2 coding rate, the mathematical model for the encoder is given by the following equation:

$$z_{\min}^{1/2}(R_b, f_{\max}) = \begin{cases} 16.32\, e^{\frac{777}{f_{\max}}(R_b - 0.0074 f_{\max})} & \text{where } 0.0074 f_{\max} \\ & \leq R_b \leq 0.013 f_{max} \\ 0 & \text{else.} \end{cases} \tag{11}$$

Since $fmax$ depends onv_{dd}, z_{min} depends on (R_b and v_{dd}) similar to equation (2). It is not necessary for the design process to develop the mathematical models because the results used are obtained from experiments; however, equations like (10 & 11) further explain the dependence of (z_{min}) on v_{dd} and bit rate as in equation (2).

3.3 Power allocation

As discussed in Section II, the bit error rate is controlled by three parameters: one is the interleaver size, the second is the encoder complexity, and the last is the transmission power. The total power consumed by a transmitting unit is given by:

$$P_T = P_C + P_N + P_t \tag{12}$$

Where P_C represents the coding power, P_N represents the interleaver power, and P_t represents the transmission power. The power consumed by the interleaver does not depend on interleaver size, as discussed above in section III, so the overall bit-error rate is not affected by the allocated power to the interleaving process. However, the allocated power to the interleaving process does affect the overall bit rate. Here, the discussion of minimizing the distortion will now only be limited to power allocation to transmission and coding processes. Let:

$$G(z_{min}, H) = \left. \frac{H^{2z_{min}+2}}{1 - H^{z_{min}-2}} \right|_{H=e^{-R_c E_b/N_0}} \tag{13}$$

Considering equation (1), power allocation for minimizing distortion must be based on minimizing $G(z_{min}, H)$. In equation (13), E_b is the received (energy/bit). It will be shown by E_b^r in the coming text. In [5] the relationship be-tween E_b^r and E_b^t (transmitted energy/bit) is given by:

$$E_b^r = h \times d^{-n} \times E_b^t$$

$$E_b^r = h \times d^{-n} \times P_t \times R_C/R_b \tag{14}$$

Where d in the above equation is the transmission distance, n is known as the path loss exponent, and the value of n is 2. In general

$$h = \frac{G_t G_r \lambda^2}{(4\pi)^2 k} \tag{15}$$

In Equation (15), h is directly proportional to the transmitter antenna gain G_t and receiver antenna gain G_r. Also directly proportional to the square of λ (transmission wavelength), but inversely proportional to k (system loss factor). If P_{max} is the power for the transmission and coding process, then:

$$P_t = Pmax - P_C \tag{16}$$

From Eq. (4):

$$P_t = P_{max} - \alpha v_{dd}^2 \tag{17}$$

Since (v_{dd}) is the parameter controlling the coding power, our aim is to select a value of (v_{dd}) such that it minimizes the equation:

$$G(z_{min}, H) = \left. \frac{H^{2z_{min}(R_b, v_{dd})+2}}{1 - H^{z_{min}(R_b, v_{dd})-2}} \right|_{H=e^{-R_c E_b^r (P_t = P_{max} - P_C)/N_0}} \tag{18}$$

By putting (z_{min} & E_b^r) values from equations (10), (11) and (17) respectively into equation (18), obtaining an explicit solution to find the value of v_{dd} at the point of minima is not possible. Therefore, graphical methods should be chosen. For $DSP(BF - 537)$ chosen as model, the equation (18) values against v_{dd} values are graphically represented in Figure (10) for a test scenario for coding rate (1/3). The graph clearly shows that the value of $G(z_{min}, H)$ is minimized at $(v_{dd} = 1.045V)$.

The antenna or chip ratings in some cases limit the values of either transmitted power (P_t) or coding power (P_C). Hence, there is a limitation on the allocation of power to the coding or transmission process. Let us suppose the coding power possible to a maximum of $(P_{C_{max}})$ and the voltage corresponding be $(v_{dd_{max}})$. Let $(v_{dd_{G,min}})$ be the supply voltage at which the distortion is minimum. If $(v_{dd_{G,min}} < v_{dd_{max}})$, then $(v_{dd_{G,min}})$ should be selected in the design. However, if the $(v_{dd_{G,min}})$ value comes out to be larger than $v_{dd_{max}}$, then $v_{dd} = v_{dd_{max}}$ be selected and $P_t = P_{max} - P_c$. The procedure is reversed if the value P_t is limited.

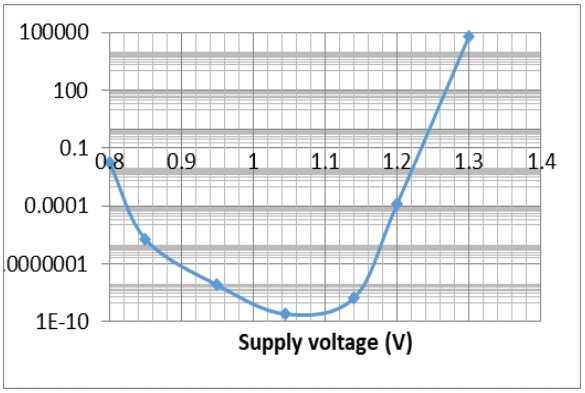

Fig. 10: The value of the expression (18) in relation to supply voltage

4 Conclusion

A design-time scheme is presented in this paper for the allocation of power between transmission and channel coding. Dynamic voltage scaling (DVS) is used for the variation of computational power. Bit rate constraints are also dealt with in this paper. With the aim of distortion minimization, the work is intended for transmission in sensor networks. Our main results are summarized as follows:

- The coding rate should be chosen based on the bit rate constraints and the available transmission bandwidth.
- The maximum bit rate achievable at a constant interleaver size for different voltage levels should be obtained, as the interleaver size does not affect the required power.
- The achievable bit rates for different optimal encoders with increasing constraint lengths at different levels of supply voltage should be determined experimentally for the available platform. In other words model should be developed for $z_{min}(R_b, v_{dd})$.
- The voltage supply should be tuned for the interleaver block for the given requirement for the bit rate. The bit rate should be supported by both the interleaver as well the convolutional encoder. The interleaver should be operated at the maximum possible core frequency for the given voltage.
- A value of voltage supply should be selected for which the value $G(z_{min}, H)$ becomes minimum. The maximum core frequency for the given voltage supply value should be used.

In the future, the work can be extended to the application of PCCC multi-user and MIMO (Multiple Input Multiple Output) scenarios to enhance spectral efficiency and robustness against interference.

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